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# A Dynamic Filter Architecture for Low Power Consumption

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*Abstract* - **The paper presents an architectural approach to the design of low power reconfigurable finite impulse response (FIR) filter. The approach is well suited when the filter order is fixed and not changed for particular applications, and efficient trade-off between power savings and filter performance can be made using the proposed architecture. Generally, FIR filter has large amplitude variations in input data and coefficients. Considering the amplitude of both the filter coefficients and inputs, the proposed FIR filter dynamically changes the filter order. Mathematical analysis on power savings and filter performance degradation and its experimental results show that the proposed approach achieves significant power savings without seriously compromising the filter performance. The power savings is up to 20.5% with minor performance degradation, and the area overhead of the proposed scheme is less than 5.3% compared to the conventional approach.**

*Keywords* – **Approximate Filtering, Low Power Filter, Reconfigurable Design, High Speed Filter.**

## I. INTRODUCTION

The demand for low power digital signal processing (DSP) systems has increased due to explosive growth in mobile computing and portable multimedia applications. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as the following equation:

$$y(n) = \sum_{k=0}^{N-1} c_k x(n-k)$$

where N represents the length of FIR filter, c*k* the *kth* coefficient, and *x(n – k)* the input data at time instant *(n - k)* . In many applications, in order to achieve high spectral containment and/or noise attenuation, FIR filters with fairly large number of taps are necessary. Many previous efforts for reducing power consumption of FIR filter generally focus on the optimization of the filter coefficients while maintaining a fixed filter order [1]–[3]. In those approaches, FIR filter structures are simplified to add and shift operations, and minimizing the number of additions/subtractions is one of the main goals of the research. However, one of the drawbacks encountered in those approaches is that once the filter architecture is decided, the coefficients cannot be changed; therefore, those techniques are not applicable to the FIR filter with programmable coefficients. Approximate signal processing techniques [4] are also used for the design of low power digital filters [5], [6]. In [5], filter order dynamically varies according to the stopband energy of the input signal. However, the approach suffers from slow filter-order adaptation time due to energy computations in the feedback mechanism. Previous studies in [6] show that sorting both the data samples and filter coefficients before the convolution operation has a desirable energy-quality characteristic of FIR filter. However, the overhead associated with the real-time sorting of incoming samples is too large. Reconfigurable FIR filter architectures are previously proposed for low power implementations [7]–[9] or to realize various frequency responses using a single filter [10]. For low power architectures, variable input word-length and filter taps [7], different coefficient word-lengths [8], and dynamic reduced signal representation [9] techniques are used. In those works, large overhead is incurred to support reconfigurable schemes such as arbitrary nonzero digit assignment [7] or programmable shift [8]. In this paper, we propose a simple yet efficient low power reconfigurable FIR filter architecture, where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply canceled. The filter performance degradation can be minimized by controlling the error bound as small as the quantization error or signal to noise power ratio (SNR) of given system. The primary goal of this work is to reduce the dynamic power of the FIR filter, and the main contributions are summarized as follows. 1) A new reconfigurable FIR filter architecture with real-time input and coefficient monitoring circuits is presented. Since the basic filter structure is not changed, it is applicable to the FIR filter with programmable coefficients or adaptive filters. 2) We provide mathematical analysis of the power saving and filter performance degradation on the proposed approach. The analysis is verified using experimental results, and it can be used as a guideline to design low power reconfigurable filters. The rest of the paper is organized as follows. In Section II, the basic idea of the proposed reconfigurable filter is described. Section III presents the reconfigurable hardware architecture and circuit techniques used to implement the filter. Discussions on the design considerations and mathematical analysis of the proposed reconfigurable FIR filter are presented in Section IV. Section V shows the numerical results, followed by conclusions in Section VI.

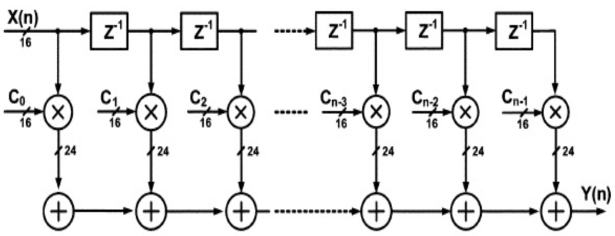


Fig.1. Architecture of the direct from FIR filter.

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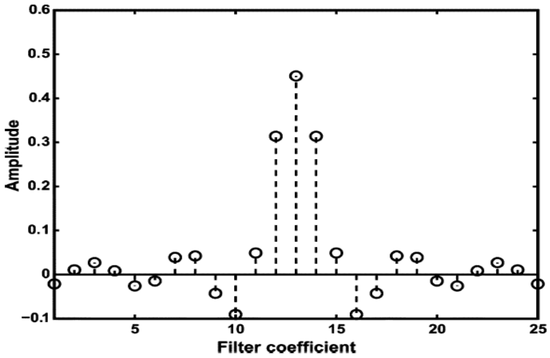



Fig.2. Amplitude of the 25-tap equi-ripple filter coefficients.

## II. Reconfigurable FIR Filtering to Trade off Filter Performance and Computation Energy

As shown in Fig. 1, FIR filtering operation performs the weighted summations of input sequences, called as convolution sum, which are frequently used to implement the frequency selective—low-pass, high-pass, or band-pass—filters. Generally, since the amount of computation and the corresponding power consumption of FIR filter are directly proportional to the filter order, if we can dynamically change the filter order by turning off some of booth's multipliers, significant power savings can be achieved. However, performance degradation should be carefully considered when we change the filter order. Fig. 2 exemplary shows the coefficients of a typical 25-tap low-pass FIR filter. The central coefficient has the largest value—the coefficient c12 has the largest value in the 25-tap FIR filter—and the amplitude of the coefficients generally decreases as becomes more distant from the center tap. The data inputs of the filter, which are multiplied with the coefficients, also have large variations in amplitude. Therefore, the basic idea is that if the amplitudes of both the data input and filter coefficient are small, the multiplication of those two numbers is proportionately small; thus, turning off the booth's multiplier has negligible effect on the filter performance. For example, since two's complement data format is widely used in the DSP applications, if one or both of the booth's multiplier input has negative value, multiplication of two small values gives rise to large switching activities, which is due to the series of 1's in the MSB part. By canceling the multiplication of two small numbers, considerable power savings can be achieved with negligible filter performance degradation. In the fixed point arithmetic of FIR filter, full operand bitwidths of the booth's multiplier outputs is not generally used. In other words, as shown in Fig. 1, when the bit-widths of data inputs and coefficients are 16, the booth's multiplier generates 32-bit outputs. However, considering the circuit area of the following adders, the LSBs of booth's multipliers outputs are usually truncated or rounded off, (e.g., 24 bits are used in Fig. 1) which incurs quantization errors. When we turn off the booth's multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible. In the following, we denote threshold of input and threshold of coefficient as *xth* and *cth*, respectively. By threshold, we mean that when the filter input *x(n)* and coefficient *ck* are smaller than *xth* and *cth* , respectively, the multiplication is canceled in the filtering operation. When we determine *xth* and *cth* , the trade-off between filter performance and power savings should be carefully considered.

## III. Reconfigurable FIR Filter Architecture

In this section, we present a direct form (DF) architecture of the reconfigurable FIR filter, which is shown in Fig. 3(a). The speed of the filter can be increased significantly, by replacing the conventional multiplier by a booth's multiplier. In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Fig. 3(b) is used. When the absolute value of *x(n)* is smaller than *xth* the threshold , the output of AD is set to “1”. The design of AD is dependent on the input threshold *xth*, where the fanin's of AND and OR gate are decided by *xth*. If and have to be changed adaptively due to designer's considerations, AD can be implemented using a simple comparator.

Dynamic power consumption of CMOS logic gates is a strong function of the switching activities on the internal node capacitances. In the proposed reconfigurable filter, if we turn off the booth's multiplier by considering each of the input amplitude only, then, if the amplitude of input *x(n)* abruptly changes for every cycle, the booth's multiplier will be turned on and off continuously, which incurs considerable switching activities. Booth's multiplier control signal decision window (MCSD) in Fig. 3(a) is used to solve the switching problem. Using *ctrl* signal generator inside MCSD, the number of input samples consecutively smaller than *xth* are counted and the booth's multipliers are turned off only when *m* consecutive input samples are smaller than *xth*. Here, *m* means the size of MCSD [in Fig. 3(a), is equal to 4].

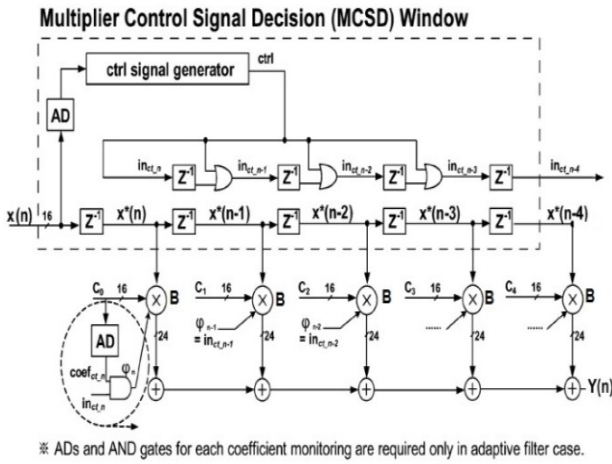



Fig.3. (a) Proposed reconfigurable FIR filter architecture.

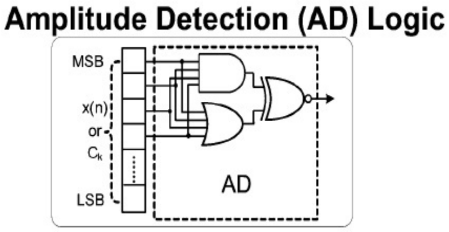
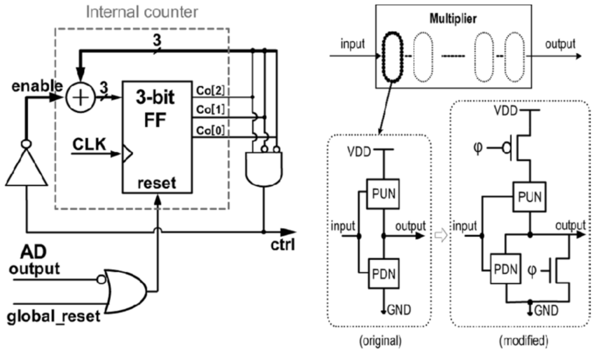



Fig.3. (b) Amplitude detection logic (AD)

Fig. 4(a) shows the *ctrl* signal generator design. As an input smaller than *xth* comes in and AD output is set to "1", the counter is counting up. When the counter reaches *m*, the *ctrl* signal in the figure changes to "1", which indicates that *m* consecutive small inputs are monitored and the booth's multipliers are ready to turn off. One additional bit *inct_n*, in Fig. 3(a), is added and it is controlled by *ctrl*. The *inct_n* accompanies with input data all the way in the following flip-flops to indicate that the input sample is smaller than *xth* and the multiplication can be canceled when the coefficient of the corresponding booth's multiplier is also smaller than *cth*. Once the *inct_n* signal is set inside MCSD, the signal does not change outside MCSD and holds the amplitude information of the input. A delay component is added in front of the first tap for the synchronization between *x*(n)* and *inctn* in Fig. 3(a) since one clock latency is needed due to the counter in MCSD. In case of adaptive filters, additional ADs for monitoring the coefficient amplitudes are required as shown in Fig. 3(a). However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed. extra AD modules for coefficient monitoring are not needed. When the amplitudes of input and coefficient are smaller than and, respectively, the booth's multiplier is turned off by setting $\varphi_n$ signal [Fig. 3(a)] to "1". Based on the simple circuit technique [11] in Fig. 4(b), the booth's multiplier can be easily turned off and the output is forced to "0". As shown in the figure, when the control signal $\varphi_n$ is "1", since PMOS turns off and NMOS turns on, the gate output is forced to "0" regardless of input. When $\varphi_n$ is "0", the gate operates like standard gate. Only the first gate of the booth's multiplier is modified and once the is set to "1", there is no switching activity in the following nodes and booth's multiplier output is set to "0". The area overheads of the proposed reconfigurable filter are flip-flops for *inct_n* signals, AD and *ctrl* signal generator inside MCSD and the modified gates in Fig. 4(b) for turning off booth's multipliers. Those overheads can be implemented using simple logic gates, and a single AD is needed for input *x(n)* monitoring as specified in Fig. 3(a). Consequently, the overall circuit overhead for implementing reconfigurable filter is as small as a single booth's multiplier.

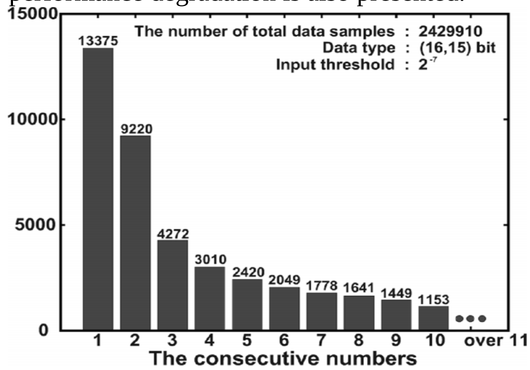


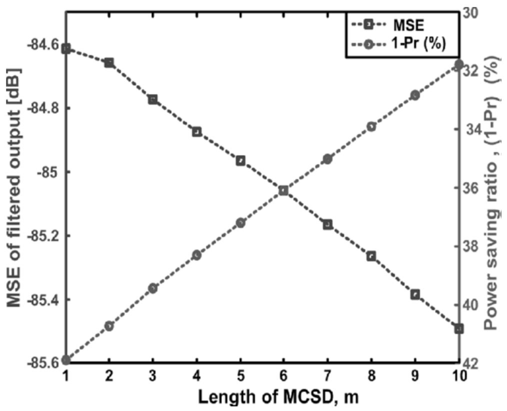

(a) (b)

Fig.4. (a) Schematic of ctrl signal generator. Internal counter sets ctrl signal to "1" when all input samples inside MCSD are smaller than xth (m = 4 case).
(b) Modified gate schematic to turn off booth's multiplier.

## IV. Design Considerations and Mathematical Analysis on the Reconfigurable FIR Filter

In this section, we present design considerations on the proposed reconfigurable FIR filter. Mathematical analysis which describes the trade-off between power savings and filter performance degradation is also presented.




### A. Design Considerations

In following discussions, as a metric of power savings, we use the power consumption ratio, P*r*, which means the ratio of the reconfigurable filter power consumption to the conventional filter power (*Preconf/Pconven*). As a measure of filter performance degradation, we use mean-square error (MSE) between the proposed reconfigurable filter output and original filter output. The most important

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factors that have a large effect on the proposed filter performance and power consumption are *xth* and *cth* . When *xth* and *cth* are set too large, it can give rise to large power savings with considerable distortion in the filter output. On the other hand, if *xth* and *cth* are too small, power savings become trivial.

The other one to be considered is *m* , the length of MCSD. Fig. 5 shows the number of input samples whose *m*(*x* axis) consecutive input values are smaller than input threshold. The input signals used in the simulation are more than ten samples of sounds and speeches. In Fig. 5, if we choose a specific value in the axis, the total number of canceled multiplications is the accumulated number of samples from the selected value to the right. Therefore, if *m* becomes larger, the number of input samples that make booth's multipliers turned off decreases; then, power reduction becomes smaller and filter performance degradation becomes lower as well. Fig. 6 shows the trade-off between the power saving ratio *(1 - Pr)* and the MSE for different *m* values in case of a 75-tap equi-ripple filter with *xth* and *cth* of $2^{-7}$.

### B. Mathematical Analysis

Mathematical modelings on the power savings and performance degradation of the proposed reconfigurable FIR filter are presented in this subsection. Detailed derivations can be found in the Appendix. Assuming the input signal as stationary random Markov process as commonly used in communication systems [12], where the future state is independent of its past states and conditionally dependent only on the present state, power saving ratio, *(1 - Pr)* , can be expressed as,

$$1 - P_r = \Pr_c \Pr_x P_{cut2cut}^{m-1}$$

Where $Prc$ $(= Pr\{\,|\,ck\,| \le cth\,\})$ and

$Prx$ $(= Pr\{\,|\,x\,(n-k\,)\,| \le xth\})$

are the probability that the amplitude of the coefficient and input signal are less than the given thresholds, i.e., $ck \le cth$ ,and $|\,x\,(n-k\,) \le xth\,|$, respectively. $Pcut2cut$ is the conditional probability meaning that future state of input samples is smaller than *xth* under present state being also smaller than *xth* ,

$$\text{i.e., } \Pr\{|x(n)| \le x_{th} \big| |x(n-1)| \le x_{th}\}, \forall\, n$$

note that power savings of the proposed reconfigurable filter are directly affected by the probabilities of inputs and coefficients being smaller than *xth* and *cth* , respectively, as well as the conditional probability. $Pcut2cut$ which is dependent upon time correlation characteristics of the input signal. It is also a function of the MCSD window size *m*. As a metric of filter performance degradation, the MSE of the filter output $\sigma_e^2$ is described as,

$$\sigma_e^2 = \Pr_c^2 \sigma_x^2 \sum_{\substack{k=0 \\ k \in C_{tc}}}^{N-1} \sum_{\substack{h=0 \\ h \in C_{tc}}}^{N-1} \times c_h c_k r_x(h-k) prob_{cut}\left(x_{th} |h-k|, m\right)$$

Where $\sigma_x^2$ $(= \mathrm{E}\{x^2(n)\})$ is the average input signal power, $r_x(\,h-k\,)$ is time correlation of input signal spaced by $(\,h-k\,)$, and $k \in C_{tc}$ denotes a set of $k$ where the $k_{\text{th}}$ filter coefficient is smaller than $c_{\text{th}}$ , i.e, $|c_k| \le c_{th}$. .

Here, $\text{prob}_{\text{cut}}\,(x_{th}\,,\,|\,h-k\,|\,,\,m)$ is the probability that the input samples at *(n-h)*, *(n-h-1),…,(n-h-m+1)* and *(n-k)*, *(n-k-1),…,(n-k-m+1)* are smaller than $x_{th}$, which is represented as ,

$$prob_{cut}(x_{th}, |h-k|, m) \approx \begin{cases} \Pr_x P_{cut2cut}^{m-1}, & when\ |h-k| > m \\ \Pr_x P_{cut2cut}^{|h-k|+(m-1)}, & when\ |h-k| \le m. \end{cases}$$

Above equation shows that the MSE is mainly determined by the filter coefficient, input signal power, auto-correlation of the input signal, and probability of input samples being smaller than $x_{th}$.

## V. Numerical Results

In this section, we have designed and implemented various types of reconfigurable FIR filters. Mathematical analysis in the previous section are verified by comparing with the experimental results.

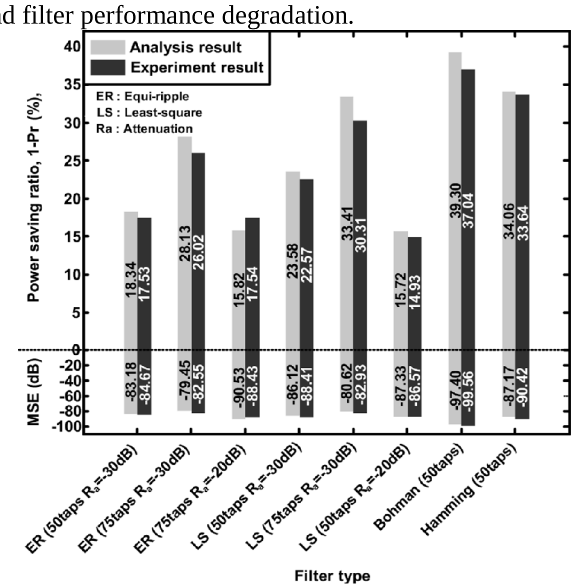
### A. Reconfigurable FIR Filter Specifications

Following are the specifications on the FIR filters implemented.

- Input sequence and coefficients are 16-bit data with fractional part of 15 bit. Hence, the data range is [-1,1]
- The outputs of the booth's multiplier in the FIR filter are quantized into 16 bit and the final filter output is 24 bit.
- We use $2^{-7}$ as an input threshold, $x_{th}$, and coefficient threshold, $c_{th}$. The values of MCSD window length, *m*, are differently assigned for the filters. The values of $x_{th}$ , $c_{th}$ and can be controlled by users considering the performance degradation and power savings trade-off presented in Section IV-B.

### B. Numerical Results

The proposed reconfigurable FIR filters are verilog coded and synthesized using TSMC 0.25µm CMOS technology. The first gate of each of the booth's multipliers is replaced with the modified gates as shown in Fig. 4(b). Power consumption is measured in the spice level simulations using [13] with the operation frequency of 100-MHz, 2.5-V supply voltage. Table I shows the average power saving ratio for the implemented FIR filters.. MSE values in the table II clearly show the minor degradation in the filter performance. Our mathematical analysis on power saving and filter performance degradation.



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(MSE) was also compared with the experimental results for various reconfigurable filters as seen in Fig. 7. We can notice from the figure that the differences between the mathematical modeling and experimental results are very small. To analyze the filter performance degradation, we define signal power to MSE ratio of the filter output (SMR) considering the effective ratio of the desired signal and the distorted error signal power as

$$SMR = \frac{\sigma_y^2}{\sigma_e^2} \approx \frac{\sum_{k=0}^{N-1}\sum_{k=0}^{N-1} c_k c_h r(h-k)}{\Pr_c^2 \sum_{\substack{k=0 \\ k \in C_{tc}}}^{N-1} \sum_{\substack{h=0 \\ h \in C_{tc}}}^{N-1} \times c_h c_k r_x(h-k) prob_{cut}\left(x_{th} \middle| h-k \middle|, m\right)}$$

Table II also presents the SMR results of various filters. For most of the cases, the SMR is larger than 45 dB, meaning that MSE is almost ignorable. For given applications, if SMR is comparable or larger than the signal to quantization error power ratio or the SNR of a given system, which are usually less than 30 dB [12], the performance degradation of proposed reconfigurable FIR filter can be considered negligible. The area overhead to support the proposed reconfigurable scheme is around 5.3% in case of 25-tap filter and it is even smaller for 50 and 75-tap filters, which are shown in Table II Fig. 8 also illustrates the filter order changes due to canceling multiplications according to the input samples' amplitudes.. Power saving ratio of each filter is normalized with the number of taps, the precision of input samples and coefficients, process technology, supply voltage, and clock frequency using the following equation [7]:

$$P(tap) = \frac{Total\ power}{\#taps} \times \frac{16}{\#bits\ coeff} \times \frac{16}{\#bits\ sample} \times \left(\frac{2.5}{Vdd}\right)^2 \times \frac{0.25}{Tech} \times \frac{100}{Clk\ freq}$$

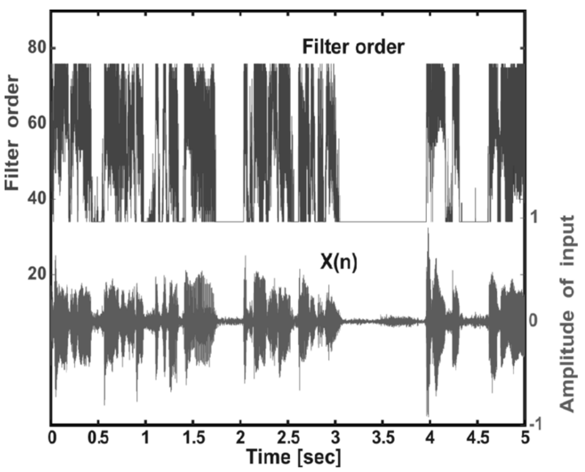


Table I

| Filter parameters | Delay | Power consumption | % increase in area | % increase in speed | Power saving % |
|---|---|---|---|---|---|
| Existing system | 4.210ns | 334mW | 5.3% | 4.67% | 15% |
| Proposed system | 4.015ns | 285mW | | | |

Our proposed filter shows larger power savings than the filters in [7] and [9]. The reconfigurable filter in [5] consumes less power than our proposed filter; however, MSE is even larger. Under the similar $1 - P_r$ obtained by adjusting parameter values, our proposed filter has much less MSE. Phonetic signal processing system is a good application to use the proposed reconfigurable filtering approach. Voice signal is usually composed of

Table II: Average power saving ratio (1-*pr*) (%), the average MSE and SMR for various filter types in speech signal case

| type | $m$ | $1\text{-}P_r$ (%) | MSE (dB) | SMR (dB) |
|---|---|---|---|---|
| | 25taps ($\omega_p$ = 0.10, $\omega_s$= 0.38, $R_a$ = -70dB) | | | |
| Equi-ripple | 3 | 19.18% | -88.74 | 49.30 |
| Least-squares | 3 | 19.78% | -88.76 | 49.32 |
| | 25taps ($\omega_p$ = 0.10, $\omega_s$= 0.20, $R_a$ = -30dB) | | | |
| Equi-ripple | 3 | 7.61% | -95.12 | 55.34 |
| Least-squares | 3 | 7.02% | -94.33 | 54.54 |
| | 25taps ($\omega_p$ = 0.10, $\omega_s$= 0.20, $R_a$ = -20dB) | | | |
| Equi-ripple | 3 | 14.68% | -92.17 | 51.86 |
| Least-squares | 3 | 7.02% | -93.61 | 53.90 |
| | 25taps ($\omega_c$ = 0.12) | | | |
| Hamming | 4 | 24.54% | -91.42 | 51.63 |
| Bohman | 3 | 24.94% | -99.56 | 59.79 |
| | 50taps ($\omega_p$ = 0.10, $\omega_s$= 0.26, $R_a \simeq$ -70dB) | | | |
| Equi-ripple | 3 | 31.84% | -88.29 | 48.75 |
| Least-squares | 3 | 31.83% | -88.49 | 48.95 |
| | 50taps ($\omega_p$ = 0.10, $\omega_s$= 0.155, $R_a \simeq$ -30dB) | | | |
| Equi-ripple | 3 | 17.53% | -84.67 | 45.16 |
| Least-squares | 3 | 22.57% | -88.41 | 48.79 |
| | 50taps ($\omega_p$ = 0.10, $\omega_s$= 0.13, $R_a \simeq$ -20dB) | | | |
| Equi-ripple | 3 | 9.73% | -94.22 | 54.92 |
| Least-squares | 3 | 14.93% | -86.57 | 46.96 |
| | 50taps ($\omega_c$ = 0.12) | | | |
| Hamming | 4 | 33.64% | -90.42 | 50.72 |
| Bohman | 3 | 37.04% | -86.47 | 46.75 |
| | 75taps ($\omega_p$ = 0.10, $\omega_s$= 0.20, $R_a \simeq$ -70dB) | | | |
| Equi-ripple | 3 | 39.45% | -84.77 | 45.19 |
| Least-squares | 3 | 41.19% | -86.29 | 46.71 |
| | 75taps ($\omega_p$ = 0.10, $\omega_s$= 0.135, $R_a \simeq$ -30dB) | | | |
| Equi-ripple | 5 | 26.02% | -82.55 | 42.71 |
| Least-squares | 5 | 30.31% | -82.93 | 43.25 |
| | 75taps ($\omega_p$ = 0.10, $\omega_s$= 0.12, $R_a \simeq$ -20dB) | | | |
| Equi-ripple | 3 | 17.64% | -88.43 | 48.60 |
| Least-squares | 5 | 28.60% | -80.20 | 40.57 |
| | 75taps ($\omega_c$ = 0.12) | | | |
| Hamming | 4 | 41.92% | -80.78 | 41.08 |
| Bohman | 3 | 42.48% | -87.00 | 47.30 |

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$\omega_p$ : narmalized passband, $\omega_s$ :stopband attenuation,

$\omega_c$ : cut – off frequency, $R_a$ :stopband attenuation

considerable portions of data samples with small amplitude. Though we focused on the FIR filters with fixed coefficients in this work, our proposed approach can be extended to the adaptive filter cases, where both data inputs and coefficients amplitude should be monitored simultaneously.

## VI. Conclusion

A low power reconfigurable FIR filter architecture allows efficient trade-off between the filter performance (in terms of area increase) and computation energy. In the proposed architecture, the input data are monitored and the multipliers in the filter are turned off when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Numerical results show that the proposed scheme achieves considerable power savings with less than around 5.34% of area overhead with very graceful degradation in the filter output. The proposed approach can be applicable to other areas of signal processing, where a proper trade-off between power savings and performance degradation should be carefully considered. Filters have 2 uses: Signal Seperation and restoration. The idea presented in this paper can assist in the design of FIR filters and its implementation for low power applications.

## Appendix

In the Appendix, we show the detail derivations of power savings and MSE of the proposed reconfigurable FIR filter.

*Power Saving Analysis:* Since turning-off multiplier in each tap can be regarded as Bernoulli random variable , turning off inside the proposed filter is binomial random variable. As a result, the power saving ratio is equal to the probability that turning-off happens. Assume that input signal as stationary Markov process,,the power saving ratio can be represented as,

$$\begin{aligned}1-P_r &= \Pr\{|c_k| \le c_{th}\} \cdot p\Pr\{|x(n-k)| \le x_{th}, \\ &\qquad |x(n-k-1)| \\ &\qquad \le x_{th}, \ldots, |x(n-k-m+1)| \le x_{th}\} \\ &= \Pr_c \cdot prob_{cut}(x_{th}, m)\end{aligned}$$

where $prob_{cut}(x_{th},m)$ is the probability that the input signal is turned off, which can be represented by,

$$\begin{aligned}&prob_{cut}(x_{th}, m) \\ &= \Pr\{|x(n-k)| \le x_{th}, |x(n-k-1)| \le x_{th}, \ldots, \\ &\qquad |x(n-k-m+1)| \le x_{th}\} \\ &= \Pr\{|x(n-k-m+1)| \le x_{th}\} \\ &\quad \cdot \Pr\{|x(n-k-m+2)| \\ &\quad \le x_{th} \big| |x(n-k-m+1)| \le x_{th}\} \cdot \\ &\quad \cdots \Pr\{|x(n-k)| \le x_{th} \big| |x(n-k-1)| \le x_{th}\} \\ &= \Pr_x P_{cut2cut}^{m-1}\end{aligned}$$

Where, $Pr_c$ ( $= P_r\{ | c_k | \le c_{th}\}$ ) and

$Pr_x$ ( $= Pr\{ | x(n-k) | \le x_{th} \}$ ) are the probabilities that the amplitude of the coefficient and input signal are less than the given thresholds,i.e, $|c_k| \le c_{th}$ and $| x(n-k)| \le$ xth , respectively. $P_{cut2cut}$ is the conditional probability that input turn-off condition,. i.e., input is lessthan $x_{th}$, happens given that the turn-off condition occurs for the input signal represented as,

$$\begin{aligned}P_{cut2cut} &= \Pr\{|x(n)| \le x_{th} \big| |x(n-1)| \le x_{th}\}, \forall\, n \\ &= \frac{\Pr\{|x(n)| \le x_{th} \text{ and } |x(n-1)| \le x_{th}\}}{\Pr\{|x(n-1)| \le x_{th}\}}.\end{aligned}$$

Note that $P_{cut2cut}$ depends upon the characteristics of the input signal which is specific to its own applications. While the above analysis is driven for more general "partially- correlated" cases using Markov process approximation, two extreme cases can be considered for more intuitive understanding.

- Case 1: timely independent signal

$$\begin{aligned}P_{cut2cut} &= \Pr\{|x(n)| \le x_{th} \big| |x(n-1)| \le x_{th}\} \\ &= \Pr\{|x(n)| \le x_{th}\} = \Pr_x.\end{aligned}$$

- Case 2: fully correlated independent signal

$$\begin{aligned}P_{cut2cut} &= \Pr\{|x(n)| \le x_{th} \big| |x(n-1)| \le x_{th}\} \\ &= 1.\end{aligned}$$

Therefore, $prob_{cut}(x_{th},m)$ has the following inequality,

$$\Pr_x^m \le \Pr_x P_{cut2cut}^{m-1} \le \Pr_x.$$

Thus, $(1 - P_r)$ (independent) $\le$ $(1- P_r)$ (partially correlated) $\le$ $(1 - P_r)$ (fully correlated), implying that the power saving ratio also depends upon the input signal's time correlation characteristics.

*Performance Degradation (MSE) Analysis:*

$$y'(n) = \sum_{k=0}^{N-1} c'_k x'(n-k) = y(n) - \sum_{\substack{k=0 \\ k \in \Upsilon_{tc}}}^{N-1} c_k x(n-k)$$

where

$$c'_k = \begin{cases} 0, & \text{when } turn\text{-}off \\ c_k, & \text{otherwise} \end{cases}$$

$$x'(n-k) = \begin{cases} 0, & \text{when } turn\text{-}off \\ x(n-k), & \text{otherwise.} \end{cases}$$

Here, k $\epsilon$ $\Upsilon_{tc}$ denotes a case where booth's multiplier turn-off occurs at $k$, *i.e.* $c_k | \le c_{th}$, $|x(n-k)| \le x_{th}, \ldots, x(n-k-m+1) \le x_{th}$. Then, the erroring of filter output is at, i.e.,

$$e(n) = y(n) - y'(n) = \sum_{\substack{k=0 \\ k \in \Upsilon_{tc}}}^{N-1} c_k x(n-k).$$

The MSE of the filter output can be represented by,

$$\sigma_e^2 = E\{|e(n)|^2\} = E\left\{ \sum_{\substack{h=0 \\ h \in \Upsilon_{tc}}}^{N-1} c_h x(n-h) \sum_{\substack{k=0 \\ k \in \Upsilon_{tc}}}^{N-1} c_k x(n-k) \right\}$$ as

$$\begin{aligned}\sigma_e^2 &= E\Bigg\{ \Bigg( \sum_{\substack{h=0 \\ h \in C_{tc}}}^{N-1} c_h \Pr\{|c_h \le c_{th}\} \cdot \int_{-x_{th}}^{x_{th}} \int_{-x_{th}}^{x_{th}} \cdots \int_{-x_{th}}^{x_{th}} \\ &\quad x_{n-h} p\{x(n-h) = x_{n-h}, x(n-h-1) \\ &\qquad = x_{n-h-1}, \ldots, x(n-h-m+1) \\ &\qquad = x_{n-h-m+1}\} dx_{n-h} dx_{n-h-1} \cdots dx_{n-h-m+1} \Bigg)\end{aligned}$$

$$\cdot\left(\sum_{\substack{k=0\\k\in C_{tc}}}^{N-1} c_k \Pr\{|c_k \le c_{th}\} \cdot \int_{-x_{th}}^{x_{th}}\int_{-x_{th}}^{x_{th}}\cdots\int_{-x_{th}}^{x_{th}} x_{n-k} p\{x(n-k)=x_{n-k}, x(n-k-1)=x_{n-k-1},\ldots, x(n-k-m+1)=x_{n-k-m+1}\} dx_{n-k}dx_{n-k-1}\cdots dx_{n-k-m+1}\right)\Bigg\}$$

$$=\Pr_c^2 \sum_{\substack{k=0\\k\in C_{tc}}}^{N-1}\sum_{\substack{h=0\\h\in C_{tc}}}^{N-1} c_h c_k \int_{-x_{th}}^{x_{th}}\int_{-x_{th}}^{x_{th}}\cdots\int_{-x_{th}}^{x_{th}} x_{n-h}x_{h-k} \cdot p\{x(n-h)=x_{n-h},\ldots,x(n-h-m+1)=x_{n-h-m+1}, x(n-k) = x_{n-k},\ldots,x(n-k-m+1)=x_{n-k-m+1}\}dx_{n-h},\ldots dx_{n-k-m+1}$$

$$\approx \Pr_c^2\sigma_x^2 \sum_{\substack{k=0\\k\in C_{tc}}}^{N-1}\sum_{\substack{h=0\\h\in C_{tc}}}^{N-1} c_h c_k r_x(h-k) prob_{cut}(x_{th},|h-k|,m)$$

Approximating $x_{n-h}x_{n-k} = \square^2_x\, r_x(h-k)$ for a simpler closed form analysis, the MSE can be written by (13) at the bottom of the page, where represents a case when the *k*th coefficient is smaller than $c_{th}$, i.e., $|c_k| \le c_{th}$. Here, $prob_{cut}(x_{th}, h-k, m)$ is the probability that input samples are turned off both at time *(n-h)* and *(n-k)*, i.e., $p\{x(n-h) \le x_{th},\ldots, x(n-h-m+1) \le x_{th},\ldots, x(n-k-m+1) \le x_{th}\}$, which can be simplified as ,

$$prob_{cut}(x_{th},|h-k|,m) \approx \begin{cases} \Pr_x P_{cut2cut}^{m-1}, & \text{when } |h-k|>m \\ \Pr_x P_{cut2cut}^{|h-k|+(m-1)}, & \text{when } |h-k|\le m \end{cases}$$

$E\{x(n-h)x(n-k)\} = \sigma_x^2 r_x(h-k)$ is the time correlation of the input signals.

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